UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,614	02/06/2004	John M. Brennan	2-81-1-4	7750

7590 05/22/2006

Wayne L. Ellenbogen
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,614	BRENNAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25* is/are allowed.

6)☒ Claim(s) *1-7 and 9-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 30, 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 and 9-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Drake et al. (US/4,961,821).

Re claim 1, Drake et al. disclose a semiconductor device, comprising: an integrated circuit die (see Figs. 9A-9E), the integrated circuit die having at least one chamfer (i.e., a groove 37 as shown in Fig. 9D) extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides (see Fig. 9E) of the IC die, the chamfer having upper surface which is angled relative to the first and second adjacent sides, the chamfer being formed an etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 2, as applied claim 1 above, Drake et al. disclose all the claimed limitations including the limitation wherein the etching process consisting of at least one of wet etching and

reactive ion etching (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 3, as applied claim 2 above, Drake et al. disclose all the claimed limitations including the limitation wherein the wet etching comprises anisotropic etching (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 4, as applied claim 1 above, Drake et al. disclose all the claimed limitations including the limitation wherein the at least a portion of the at least one perimeter edge of the integrated circuit die is beveled by forming one or more v-shaped grooves in an upper surface of the device (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 5, as applied claim 1 above, Drake et al. disclose all the claimed limitations including the limitation wherein the angle of the upper surface of the at least one chamfer of the IC die is controlled, at least in part, by selectively varying one or more characteristics of the etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 6, as applied claim 5 above, Drake et al. disclose all the claimed limitations including the limitation wherein the one or more characteristics of the etching process comprises at least one of a type of etchant, a temperature and a duration of etching (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 7, as applied claim 1 above, Drake et al. disclose all the claimed limitations including a plurality of integrated circuit die, at least one of the integrated circuit die being separated from the semiconductor device by: (i) forming one or more v-shaped grooves in an upper surface of the device, the v-shaped grooves defining perimeter edges of the at least one integrated circuit die;, and (ii) removing a back surface of the semiconductor device opposite the

upper surface of the device until at least a portion of the v-grooves are exposed; wherein a sidewall of each of the v-shaped grooves forms a beveled perimeter edge of the separated die (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 9, as applied claim 1 above, Drake et al. disclose all the claimed limitations including the limitation wherein the IC comprises a plurality of chamfers joining a respective pair of adjacent sides of IC die and having an upper surface which is angled relative to the respective pair of adjacent sides (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 10, as applied claim 9 above, Drake et al. disclose all the claimed limitations including the limitation wherein the respective angles of the upper surfaces of the chamfers relative to corresponding pairs of adjacent sides of the IC die are substantially matched to one another (see Figs. 9A-9E; 10-11B and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 11, as applied claim 1 above, Drake et al. disclose all the claimed limitations including the limitation wherein the angle of the upper surface of the at least one chamfer in the integrated circuit die is substantially matched to an angle of a sidewall of a die collet configurable for receiving the die (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 12, as applied claim 1 above, Drake et al. disclose all the claimed limitations including the limitation wherein at least two perimeter edges of the integrated circuit die are beveled by the etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 13, as applied claim 1 above, Drake et al. disclose all the claimed limitations including the limitation wherein all perimeter edges of the integrated circuit die are beveled by the etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 14, Drake et al. disclose a method for separating at least one integrated circuit die from an associated semiconductor wafer, the method comprising the steps of: forming one or more v-shaped grooves (37) (see Fig. 9D) in an upper surface (31) of the semiconductor wafer by an etching process, the one or more v-shaped grooves defining perimeter edges of the at least one integrated circuit die (see Fig. 9D); and removing a back surface (32) of the semiconductor wafer opposite the upper surface of the wafer until at least a portion of the one or more v-shaped grooves are exposed (see Fig. 9E) ; forming least one chamfer (i.e., a groove 37 as shown in Fig. 9D) in the at least IC die, the chamfer extending form a top surface of the integrated circuit to an intersection first and second adjacent sides (see Fig. 9E) of the IC die, the chamfer having upper surface which is angled relative to the first and second adjacent sides; wherein a sidewall of each of the one or more v-grooves forms a beveled perimeter edge of the separated at least one integrated circuit die (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 15, as applied claim 14 above, Drake et al. disclose all the claimed limitations including the limitation wherein the etching process comprises anisotropic etching (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 16, as applied claim 14 above, Drake et al. disclose all the claimed limitations including the limitation the step of controlling an angle of the at least one of the upper surface of

the chamfer and the sidewall of at least one of the v-shaped grooves, at least in part, by selectively varying one or more characteristics of the etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 17, as applied claim 16 above, Drake et al. disclose all the claimed limitations including the limitation wherein the one or more characteristics of the etching process comprises at least one of a type of etchant, a temperature and a duration of etching (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 18, Drake et al. disclose a method for reducing post-fabrication surface damage to an integrated circuit die, the method comprising the step forming least one chamfer (i.e., a groove 37 as shown in Fig. 9D) in the at least IC die, the chamfer extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides (see Fig. 9E) of the IC die, the chamfer having upper surface which is angled relative to the first and second adjacent sides (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 19, as applied claim 18 above, Drake et al. disclose all the claimed limitations including the limitation the step of controlling an angle at which the at least a portion of the upper surface of the at least one chamfer by selectively varying one or more characteristics of the etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 20, as applied claim 18 above, Drake et al. disclose all the claimed limitations including the limitation wherein the step of forming the at least chamfer comprises forming one or more v-shaped grooves in an upper surface of the integrated circuit (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 21, as applied claim 18 above, Drake et al. disclose all the claimed limitations including the limitation wherein the step of forming at least one chamfer comprises the step of substantially matching the angle of the upper surface of the chamfer to an angle of at least one sidewall of a die collet configurable for receiving the die (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 22, Drake disclose a packaged integrated circuit device, comprising: at least one integrated circuit die, die having at least one chamfer (i.e., a groove 37 as shown in Fig. 9D) extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides (see Fig. 9E) of the IC die, the chamfer having upper surface which is angled relative to the first and second adjacent sides, the chamfer the at least one integrated circuit die being formed by an etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 23, as applied claim 22 above, Drake et al. disclose all the claimed limitations including the limitation wherein the at least a portion of at least one perimeter edge of the at least one integrated circuit die is beveled by forming one or more v-shaped grooves in an upper surface of the at least one integrated circuit die (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 24, as applied claim 22 above, Drake et al. disclose all the claimed limitations including the limitation wherein the angle of the upper surface of the chamfer in the at least one integrated circuit die is controlled, at least in part, by selectively varying one or more characteristics of the etching process (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Allowable Subject Matter

4. Claim 25 is allowed over prior art of record.

***Response* to Arguments**

5. Applicants' arguments filed March 30, 2006 have been fully considered but they are not persuasive.

Applicants argue that "Drake fails to teach or suggest integrated circuit die having at least on chamfer disposed at first and second adjacent sides of the IC die ..."

In response to applicants argument, it is respectfully submitted that Drake et al. '821disclose all the claimed limitations including the limitation *the integrated circuit die having at least one chamfer* (i.e., a groove 37 as shown in Fig. 9D) *extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides.*

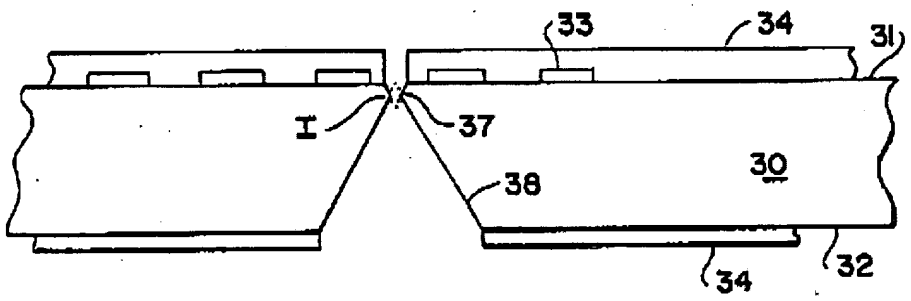

Fig- 9E

As depicted on Fig. 9E above, the chamfer (37) (i.e., upper surface) the bottom groove (38) (i.e., the bottom surface) are joined (i.e., the top and bottom sides of the IC die connected through the via and detached). In addition the chamfer 37 is angled relative to the front and the back side of the IC chip. As depicted in Fig. 9E, its clearly Drake disclose chamfer (i.e., a groove 37 as shown in Fig. 9D) extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides,

Therefore, the rejection of claims 1-24 under 35 U.S.C. 102 is deemed proper.

Conclusion

6. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
May 13, 2006